AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A device for converting data sequences between frame relay (FR) format ~~(FR)~~ and asynchronous transfer mode (ATM) format, comprising:

an FR communication module for connecting to at least one FR communication link;

an ATM communication module for connecting to an ATM communication link;

a central computer for controlling said FR communication module and said ATM communication module; and

~~a~~ buffer memory, which is connected via an internal communication link to said central computer, said FR communication module and said ATM communication link, the buffer memory ~~being configured to store~~ comprising at least one memory that stores both FR data sequences from the FR communications module and ATM data sequences from the ATM communications module, at least one of the FR data sequences and the ATM data sequences comprising usage data and control data.

2. (Previously Presented) A device according to claim 1, wherein said internal communication link comprises a bus link.

3. (Currently Amended) A device according to claim 2, wherein said bus link comprises a Peripheral Component Interconnect (PCI) bus link

4. (Previously Presented) A device according to claim 1, wherein said internal communication link comprises two separate bus links for driving said FR communication module.

5. (Previously Presented) A device according to claim 1, wherein said central computer controls data transmission between said FR communication module, said ATM communication module, said central computer and said buffer memory.

6. (Previously Presented) A device according to claim 1, wherein said buffer memory comprises a reception unit and a transmission unit.

7. (Currently Amended) A device according to claim 6, further comprising an additional central computer which controls conversion of data sequences from the FR format into the ATM format~~; wherein said additional central computer controls conversion of said data sequences from FR format into ATM format~~.

8. (Currently Amended) A method for converting data sequences from a frame relay (FR) format into an asynchronous transfer mode (ATM) format, the method comprising:

connecting an FR communication module to an FR communication link;

connecting an ATM communication module to an ATM communication link;

controlling, with a central computer, said FR communication module and said ATM communication module;

reading-in FR data sequences into said FR communication module as read-in data;

storing said read-in data in a buffer memory;

converting ~~said~~ stored read-in data into ATM format; and

reading-out said stored read-in data as read-out data converted into ATM format via said ATM communication module; ~~and~~

wherein reading-in read-in data into the buffer memory or reading-out read-out data from the buffer memory does not interrupt an operation of the central computer, and wherein the buffer memory comprises at least one memory that stores both FR data sequences and ATM data sequences, at least one of the FR data sequences and the ATM data sequences comprising usage data and control data.

9. (Currently Amended) A method for converting data sequences from an asynchronous transfer mode (ATM) format into a frame relay (FR) format comprising:

connecting ~~a~~ an FR communication module to an FR communication link;

connecting ~~a~~ an ATM communication module to an ATM communication link;

controlling, ~~with said~~ via a central computer, said FR communication module and said ATM communication module;

reading-in and desegmenting an ATM data sequence in said ATM communication module as read-in data;

storing said read-in data in a buffer memory;

converting ~~said~~ stored read-in data into FR format; and

reading out said stored read-in data as read-out data converted into FR format from said buffer memory via said FR communication module; ~~and~~

wherein reading-in read-in data into the buffer memory or reading-out read-out data from the buffer memory does not interrupt an operation of the central computer, and wherein the buffer memory comprises at least one memory that stores both FR data sequences and ATM data sequences, at least one of the FR data sequences and the ATM data sequences comprising usage data and control data.

10. (Currently Amended) A device for converting data sequences between frame relay (FR) format ~~(FR)~~ and asynchronous transfer mode (ATM) format, comprising:

an FR communication module for connecting to at least one FR communication link;

an ATM communication module for connecting to an ATM communication link;

a central computer for controlling said FR communication module and said ATM communication module; and

a buffer memory, which is connected via an internal communication link to said central computer, said FR communication module and said ATM communication link;

wherein said internal communication link comprises two separate bus links for driving said FR communication module.

11. (Previously Presented) The device of claim 10, wherein said internal communication link comprises a bus link.

12. (Currently Amended) The device of claim 11, wherein said bus link comprises a Peripheral Component Interconnect (PCI) bus link

13. (Previously Presented) The device of claim 10, wherein said central computer controls data transmission between said FR communication module, said ATM communication module, said central computer and said buffer memory.

14. (Previously Presented) The device of claim 10, wherein said buffer memory comprises a reception unit and a transmission unit.

15. (Currently Amended) A device for converting data sequences between frame relay (FR) format ~~(FR)~~ and asynchronous transfer mode (ATM) format, comprising:

an FR communication module for connecting to at least one FR communication link;

an ATM communication module for connecting to an ATM communication link;

a central computer for controlling said FR communication module and said ATM communication module;

a buffer memory, which is connected via an internal communication link to said central computer, said FR communication module and said ATM communication link; and

an additional central computer which controls conversion of data sequences from the FR format into the ATM format;

wherein said additional central computer controls conversion of said data sequences from FR format into ATM format, and wherein said buffer memory comprises a reception unit and a transmission unit

16. (Previously Presented) The device of claim 15, wherein said internal communication link comprises a bus link.

17. (Previously Presented) The device of claim 16, wherein said bus link comprises a PCI bus link

18. (Previously Presented) The device of claim 15, wherein said central computer controls data transmission between said FR communication module, said ATM communication module, said central computer and said buffer memory.

19. (Previously Presented) The method of claim 8, wherein said internal communication link comprises a bus link.

20. (Currently Amended) The method of claim 19, wherein said bus link comprises a Peripheral Component Interconnect (PCI) bus link

21. (Previously Presented) The method of claim 8, wherein said central computer controls data transmission between said FR communication module, said ATM communication module, said central computer and said buffer memory.

22. (Previously Presented) The method of claim 8, wherein said buffer memory comprises a reception unit and a transmission unit.

23. (Previously Presented) The method of claim 9, wherein said internal communication link comprises a bus link.

24. (Currently Amended) The method of claim 23, wherein said bus link comprises a Peripheral Component Interconnect (PCI) bus link

25. (Previously Presented) The method of claim 9, wherein said central computer controls data transmission between said FR communication module, said ATM communication module, said central computer and said buffer memory.

26. (Previously Presented) The method of claim 9, wherein said buffer memory comprises a reception unit and a transmission unit.